

EAST - [0249a.wsp:1]

File View Edit Tools Window Help

Pending

Active

- L1: (105) (gate with angle) with (isolat\$4)
- L2: (6) "6232635"
- L3: (128) (gate with angle) with (isolat\$4)
- L4: (51) (gate with isotropic\$5) with (isolat\$4)

Search List Browse Queue Clear

DBs: USPAT; US-PGPUB Plurals

Default operator: OR Highlight all hit terms initially

(gate with isotropic\$5) with (isolat\$4)

BRS form IS&R form Image Text HTML

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	<input type="checkbox"/>	<input type="checkbox"/>	US 20040121573 A1	20040624	10	Method for forming enhanced areal density split gate field effect transistor	438/594	438/266
2	<input type="checkbox"/>	<input type="checkbox"/>	US 20040104411 A1	20040603	10	Method for producing a gate for a cmos transistor structure having a cha	257/204	
3	<input type="checkbox"/>	<input type="checkbox"/>	US 20040072412 A1	20040415	14	Recessed gate electrode MOS transistors having a substantially unifo	438/589	257/328; 257/330;
4	<input type="checkbox"/>	<input type="checkbox"/>	US 20040043589 A1	20040304	17	Method for fabricating source/drain devices	438/585	438/595
5	<input type="checkbox"/>	<input type="checkbox"/>	US 20040038484 A1	20040226	17	METHOD FOR FABRICATING SOURCE/DRAIN DEVICES	438/286	257/E21.427; 438/305
6	<input type="checkbox"/>	<input type="checkbox"/>	US 20040021172 A1	20040205	10	Fully isolated dielectric memory cell structure for a dual bit nitride storage	257/316	257/E21.21; 257/E29.165
7	<input type="checkbox"/>	<input type="checkbox"/>	US 20040014276 A1	20040122	13	Method of making a semiconductor transistor	438/231	257/E21.634; 257/E21.636;
8	<input type="checkbox"/>	<input type="checkbox"/>	US 20040000690 A1	20040101	68	Method of manufacturing semiconductor device and semicondu	257/334	
9	<input type="checkbox"/>	<input type="checkbox"/>	US 20030211680 A1	20031113	15	Interfacial layer for gate electrode and high-k dielectric layer and methods of	438/200	257/E21.29
10	<input type="checkbox"/>	<input type="checkbox"/>	US 20030203594 A1	20031030	58	Non-volatile semiconductor memory device and manufacturing method the	438/424	257/E21.682; 257/E27.103
11	<input type="checkbox"/>	<input type="checkbox"/>	US 20030153136 A1	20030814	68	Method of manufacturing semicontor device having trench isolation	438/151	257/E21.564; 257/E21.661;
12	<input type="checkbox"/>	<input type="checkbox"/>	US 20030132525	20030717	62	Semiconductor device and its	257/773	257/774;

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	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
15	<input type="checkbox"/>	<input type="checkbox"/>	US 20030109102 A1	20030612	71	Method of manufacturing semiconductor device and semicondu	438/243	
16	<input type="checkbox"/>	<input type="checkbox"/>	US 20030096466 A1	20030522	7	Method for forming gate dielectrics of varying thicknesses on a wafer	438/197	257/E21.625; 257/E21.628;
17	<input type="checkbox"/>	<input type="checkbox"/>	US 20030049899 A1	20030313	20	Electrode structures	438/200	438/978
18	<input type="checkbox"/>	<input type="checkbox"/>	US 20030022449 A1	20030130	18	Method of manufacturing a semiconductor device having a trench	438/296	257/E21.546; 257/E21.628;
19	<input type="checkbox"/>	<input type="checkbox"/>	US 20020182806 A1	20021205	14	Nonvolatile memory device having STI structure and method of fabricati	438/257	257/E21.548; 257/E21.688;
20	<input type="checkbox"/>	<input type="checkbox"/>	US 20010018253 A1	20010830	20	Semiconductor device and manufacturing method thereof	438/296	257/E21.682; 257/E27.103
21	<input type="checkbox"/>	<input type="checkbox"/>	US 20010005620 A1	20010628	26	Process for manufacturing semiconductor device	438/584	257/E21.576; 257/E21.682;
22	<input type="checkbox"/>	<input type="checkbox"/>	US 6734492 B2	20040511	26	Nonvolatile vertical channel semiconductor device	257/316	257/315; 257/321;
23	<input type="checkbox"/>	<input type="checkbox"/>	US 6713338 B2	20040330	16	Method for fabricating source/drain devices	438/231	257/E21.427; 438/224;
24	<input type="checkbox"/>	<input type="checkbox"/>	US 6639271 B1	20031028	8	Fully isolated dielectric memory cell structure for a dual bit nitride storage	257/324	257/314; 257/327;
25	<input type="checkbox"/>	<input type="checkbox"/>	US 6636721 B2	20031021	74	Network engineering/systems system for mobile satellite communication sy	455/12.1	455/427; 455/428
26	<input type="checkbox"/>	<input type="checkbox"/>	US 6620713 B2	20030916	14	Interfacial layer for gate electrode and	438/585	257/E21.29

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	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
27	<input type="checkbox"/>	<input type="checkbox"/>	US 6566187 B1	20030520	13	DRAM cell system and method for producing same	438/239	257/E21.652; 257/E27.096;
28	<input type="checkbox"/>	<input type="checkbox"/>	US 6555427 B1	20030429	55	Non-volatile semiconductor memory device and manufacturing method the	438/238	257/314; 257/E21.682;
29	<input type="checkbox"/>	<input type="checkbox"/>	US 6544843 B2	20030408	26	Process for manufacturing semiconductor device	438/257	257/E21.576; 257/E21.682;
30	<input type="checkbox"/>	<input type="checkbox"/>	US 6538295 B1	20030325	10	Salicide device with borderless contact	257/412	257/384; 257/388;
31	<input type="checkbox"/>	<input type="checkbox"/>	US 6534355 B2	20030318	24	Method of manufacturing a flash memory having a select transistor	438/201	257/E21.685; 257/E21.688;
32	<input type="checkbox"/>	<input type="checkbox"/>	US 6455381 B1	20020924	17	Method of manufacturing a semiconductor device having a trench	438/296	257/E21.546; 257/E21.628;
33	<input type="checkbox"/>	<input type="checkbox"/>	US 6448135 B1	20020910	25	Semiconductor device and method of fabricating same	438/257	257/E21.693; 257/E27.103;
34	<input type="checkbox"/>	<input type="checkbox"/>	US 6417047 B1	20020709	19	Manufacturing method of a non-volatile semiconductor memory	438/258	257/E21.548; 438/296
35	<input type="checkbox"/>	<input type="checkbox"/>	US 6413809 B2	20020702	19	Method of manufacturing a non-volatile memory having an eleme	438/201	257/E21.682; 257/E27.103;
36	<input type="checkbox"/>	<input type="checkbox"/>	US 6410991 B1	20020625	31	Semiconductor device and method of manufacturing the same	257/392	257/607; 257/E21.625;
37	<input type="checkbox"/>	<input type="checkbox"/>	US 6348390 B1	20020219	10	Method for fabricating MOSFETS with a recessed self-aligned silicide c	438/305	257/396; 257/408;
38	<input type="checkbox"/>	<input type="checkbox"/>	US 6284637 B1	20010904	8	Method to fabricate a floating gate	438/594	257/E21.209;

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	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
39	<input type="checkbox"/>	<input type="checkbox"/>	US 6274440 B1	20010814	8	Manufacturing of cavity fuses on gate conductor level	438/281	257/E23.149; 257/E23.15;
40	<input type="checkbox"/>	<input type="checkbox"/>	US 6242317 B1	20010605	19	High quality isolation structure formation	438/400	257/E21.546; 438/788
41	<input type="checkbox"/>	<input type="checkbox"/>	US 6222225 B1	20010424	20	Semiconductor device and manufacturing method thereof	257/315	257/374; 257/506;
42	<input type="checkbox"/>	<input type="checkbox"/>	US 6175133 B1	20010116	15	Flash memory cell and method of fabricating the same	257/320	257/E21.682; 257/E27.103;
43	<input type="checkbox"/>	<input type="checkbox"/>	US 6174762 B1	20010116	11	Salicide device with borderless contact	438/230	257/413; 257/E21.438;
44	<input type="checkbox"/>	<input type="checkbox"/>	US 5973353 A	19991026	9	Methods and arrangements for forming a tapered floating gate in non	257/315	257/317; 257/508;
45	<input type="checkbox"/>	<input type="checkbox"/>	US 5946570 A	19990831	42	Process for fabricating semiconductor device having semico	438/253	257/E21.648; 438/413
46	<input type="checkbox"/>	<input type="checkbox"/>	US 5814537 A	19980929	14	Method of forming transistor electrodes from directionally deposite	438/151	148/DIG.147; 257/E21.415;
47	<input type="checkbox"/>	<input type="checkbox"/>	US 5759880 A	19980602	5	Resistless methods of fabricating FETs	438/184	257/E21.037; 257/E21.407;
48	<input type="checkbox"/>	<input type="checkbox"/>	US 5397722 A	19950314	9	Process for making self-aligned source/drain polysilicon or polysilicid	438/303	148/DIG.20; 257/E21.435;
49	<input type="checkbox"/>	<input type="checkbox"/>	US 5179032 A	19930112	15	Mosfet structure having reduced capacitance and method of forming s	438/268	148/DIG.126; 257/E21.418;
50	<input type="checkbox"/>	<input type="checkbox"/>	US 5121176 A	19920609	16	MOSFET structure having reduced	257/340	257/145;

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L1: (105) (gate with taper\$3) with (isolat\$4)								
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U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	
<input type="checkbox"/>	<input type="checkbox"/>	US 20040092057 A1	20040513	36	Semiconductor device and manufacturing method thereof	438/142	257/E21.205; 257/E21.444;	
<input type="checkbox"/>	<input type="checkbox"/>	US 20040063266 A1	20040401	22	Semiconductor device and method of manufacturing the same	438/200	257/E21.546; 257/E21.628;	
<input type="checkbox"/>	<input type="checkbox"/>	US 20030232472 A1	20031218	26	Methods of fabricating a stack-gate non-volatile memory device and its c	438/257		
<input type="checkbox"/>	<input type="checkbox"/>	US 20030209757 A1	20031113	10	Semiconductor component with an increased breakdown voltage in the e	257/329	257/E29.131; 257/E29.26	
<input type="checkbox"/>	<input type="checkbox"/>	US 20030151063 A1	20030814	12	Semiconductor device and method of fabricating semiconductor device	257/192	257/194; 257/E21.407;	
<input type="checkbox"/>	<input type="checkbox"/>	US 20030134473 A1	20030717	10	Novel process for flash memory cell	438/257		
<input type="checkbox"/>	<input type="checkbox"/>	US 20030064589 A1	20030403	12	Method for forming inside nitride spacer for deep trench device DRAM	438/689		
<input type="checkbox"/>	<input type="checkbox"/>	US 20030053345 A1	20030320	25	Nonvolatile semiconductor storage device and production method thereof	365/200	257/E21.679; 257/E27.103;	
<input type="checkbox"/>	<input type="checkbox"/>	US 20020149081 A1	20021017	92	Semiconductor device and method of fabricating the same	257/510	257/E21.679; 257/E27.103;	
<input type="checkbox"/>	<input type="checkbox"/>	US 20020034850 A1	20020321	31	Method for manufacturing a nonvolatile semiconductor memory d	438/257	257/E21.662; 257/E21.682;	
<input type="checkbox"/>	<input type="checkbox"/>	US 20020030223 A1	20020314	22	Semiconductor device and method of manufacturing the same	257/314	257/506; 257/E21.546;	
<input type="checkbox"/>	<input type="checkbox"/>	US 20020008293 A1	20020124	36	SEMICONDUCTOR DEVICE INCLUDING INVERSELY TAPER	257/412	257/E21.205; 257/E21.444;	
<input type="checkbox"/>	<input type="checkbox"/>	US 20020005562 A1	20020117	14	Semiconductor power integrated circuit and method for fabricating the	257/510	257/492; 257/E21.564;	
<input type="checkbox"/>	<input type="checkbox"/>	US 20010019508 A1	20010906	23	Nonvolatile semiconductor memory device having tapered portion on side	365/203		
<input type="checkbox"/>	<input type="checkbox"/>	US 20010019150	20010906	39	Non-volatile semiconductor memory	257/315	257/324	





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	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
31	<input type="checkbox"/>	<input type="checkbox"/>	US 6403421 B1	20020611	36	Semiconductor nonvolatile memory device and method of producing the	438/267	257/E21.682;
32	<input type="checkbox"/>	<input type="checkbox"/>	US 6365462 B2	20020402	30	Methods of forming power semiconductor devices having tapere	438/270	257/E21.103;
33	<input type="checkbox"/>	<input type="checkbox"/>	US 6342715 B1	20020129	63	Nonvolatile semiconductor memory device	257/314	257/E21.359;
34	<input type="checkbox"/>	<input type="checkbox"/>	US 6340611 B1	20020122	65	Nonvolatile semiconductor memory device	438/201	257/E21.419;
35	<input type="checkbox"/>	<input type="checkbox"/>	US 6284605 B1	20010904	13	Method for fabricating semiconductor power integrated circu	438/268	257/315;
36	<input type="checkbox"/>	<input type="checkbox"/>	US 6252271 B1	20010626	17	Flash memory structure using sidewall floating gate and method for	257/315	257/E21.564;
37	<input type="checkbox"/>	<input type="checkbox"/>	US 6228712 B1	20010508	37	Non-volatile semiconductor memory device and manufacturing method the	438/257	257/E21.703;
38	<input type="checkbox"/>	<input type="checkbox"/>	US 6222225 B1	20010424	20	Semiconductor device and manufacturing method thereof	257/315	257/316;
39	<input type="checkbox"/>	<input type="checkbox"/>	US 6191447 B1	20010220	30	Power semiconductor devices that utilize tapered trench-based insulating	257/330	257/317;
40	<input type="checkbox"/>	<input type="checkbox"/>	US 6081662 A	20000627	33	Semiconductor device including trench isolation structure and a metho	703/14	257/E21.209;
41	<input type="checkbox"/>	<input type="checkbox"/>	US 6025242 A	20000215	7	Fabrication of semiconductor device having shallow junctions including an	438/303	257/E21.682;
42	<input type="checkbox"/>	<input type="checkbox"/>	US 6022771 A	20000208	9	Fabrication of semiconductor device having shallow junctions and sidewall	438/230	257/374;
43	<input type="checkbox"/>	<input type="checkbox"/>	US 6018185 A	20000125	51	Semiconductor device with element isolation film	257/374	257/506;
44	<input type="checkbox"/>	<input type="checkbox"/>	US 5998273 A	19991207	7	Fabrication of semiconductor device having shallow junctions	438/305	257/333;
45	<input type="checkbox"/>	<input type="checkbox"/>	US 5998248 A	19991207	7	Fabrication of semiconductor device	438/231	257/471;

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	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
47	<input type="checkbox"/>	<input type="checkbox"/>	US 5949102 A	19990907	21	Semiconductor device having a gate electrode with only two crystal grains	257/315	257/153; 257/249;
48	<input type="checkbox"/>	<input type="checkbox"/>	US 5895237 A	19990420	11	Narrow isolation oxide process	438/225	257/E21.435; 257/E21.557;
49	<input type="checkbox"/>	<input type="checkbox"/>	US 5874328 A	19990223	11	Reverse CMOS method for dual isolation semiconductor device	438/199	257/E21.551; 257/E21.642;
50	<input type="checkbox"/>	<input type="checkbox"/>	US 5828120 A	19981027	67	Semiconductor device and production method thereof	257/499	257/401; 257/506;
51	<input type="checkbox"/>	<input type="checkbox"/>	US 5801082 A	19980901	8	Method for making improved shallow trench isolation with dielectric studs f	438/424	148/DIG.50; 257/E21.551;
52	<input type="checkbox"/>	<input type="checkbox"/>	US 5712491 A	19980127	8	Lateral theta device	257/26	257/29; 257/E29.042;
53	<input type="checkbox"/>	<input type="checkbox"/>	US 5711509 A	19980127	14	Isolation gate and frame assembly	251/175	251/193; 251/328
54	<input type="checkbox"/>	<input type="checkbox"/>	US 5516710 A	19960514	14	Method of forming a transistor	438/309	257/E21.375; 257/E21.507;
55	<input type="checkbox"/>	<input type="checkbox"/>	US 5502320 A	19960326	42	Dynamic random access memory (DRAM) semiconductor device	257/302	257/301; 257/329;
56	<input type="checkbox"/>	<input type="checkbox"/>	US 5356823 A	19941018	9	Method of manufacturing a semiconductor device	438/180	148/DIG.131; 257/E21.234;
57	<input type="checkbox"/>	<input type="checkbox"/>	US 5248636 A	19930928	80	Processing method using both a remotely generated plasma and an in-	438/709	216/63; 216/67;
58	<input type="checkbox"/>	<input type="checkbox"/>	US 5138973 A	19920818	82	Wafer processing apparatus having independently controllable energy sou	118/723MP	118/719; 118/723E;
59	<input type="checkbox"/>	<input type="checkbox"/>	US 4988533 A	19910129	83	Method for deposition of silicon oxide on a wafer	427/563	427/294; 427/572;
60	<input type="checkbox"/>	<input type="checkbox"/>	US 4949671 A	19900821	82	Processing apparatus and method	118/725	118/715
61	<input type="checkbox"/>	<input type="checkbox"/>	US 4944488 A	19900731	9	Gate valve	251/203	251/214



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61	<input type="checkbox"/>	<input type="checkbox"/>	US 4944488 A	19900731	9	Gate valve	251/203	251/214; 251/329
62	<input type="checkbox"/>	<input type="checkbox"/>	US 4923562 A	19900508	81	Processing of etching refractory metals	216/67	204/192.35; 216/75;
63	<input type="checkbox"/>	<input type="checkbox"/>	US 4915777 A	19900410	81	Method for etching tungsten	438/711	252/79.1; 257/E21.311;
64	<input type="checkbox"/>	<input type="checkbox"/>	US 4911103 A	19900327	81	Processing apparatus and method	118/725	118/715; 118/728;
65	<input type="checkbox"/>	<input type="checkbox"/>	US 4910043 A	19900320	81	Processing apparatus and method	427/563	118/722; 118/723ME;
66	<input type="checkbox"/>	<input type="checkbox"/>	US 4906328 A	19900306	82	Method for wafer treating	438/694	427/299; 427/399;
67	<input type="checkbox"/>	<input type="checkbox"/>	US 4904621 A	19900227	83	Remote plasma generation process using a two-stage showerhead	134/1.2	118/50.1; 118/620;
68	<input type="checkbox"/>	<input type="checkbox"/>	US 4891488 A	19900102	82	Processing apparatus and method	219/121.4	118/709; 156/345.43;
69	<input type="checkbox"/>	<input type="checkbox"/>	US 4889492 A	19891226	9	High capacitance trench capacitor and well extension process	438/390	257/E21.396; 257/E21.544;
70	<input type="checkbox"/>	<input type="checkbox"/>	US 4886570 A	19891212	83	Processing apparatus and method	438/711	118/50.1; 156/345.35;
71	<input type="checkbox"/>	<input type="checkbox"/>	US 4877757 A	19891031	83	Method of sequential cleaning and passivating a GaAs substrate using re	438/767	134/1.2; 148/DIG.17;
72	<input type="checkbox"/>	<input type="checkbox"/>	US 4875989 A	19891024	82	Wafer processing apparatus	204/298.33	156/345.33; 156/345.37;
73	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 4874723 A	19891017	83	Selective etching of tungsten by remote and in situ plasma generation	438/696	118/620; 148/DIG.51;
74	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 4872938 A	19891010	83	Processing apparatus	156/345.54	118/729
75	<input type="checkbox"/>	<input type="checkbox"/>	US 4867841 A	19890919	81	Method for etch of polysilicon film	438/711	257/E21.312;

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76	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 4863558 A	19890905	81	Method for etching tungsten	438/695	438/720
77	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 4857132 A	19890815	83	Processing apparatus for wafers	156/345.33	118/50.1; 438/935
78	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 4855160 A	19890808	83	Method for passivating wafer	438/767	204/192.1; 257/E21.493;
79	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 4855016 A	19890808	84	Method for etching aluminum film doped with copper	438/710	257/E21.311; 438/720
80	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 4849067 A	19890718	81	Method for etching tungsten	216/75	257/E21.311
81	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 4844773 A	19890704	83	Process for etching silicon nitride film	438/711	257/E21.252; 438/719;
82	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 4842687 A	19890627	82	Method for etching tungsten	438/711	252/79.1; 257/E21.234;
83	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 4842686 A	19890627	85	Wafer processing apparatus and method	438/709	156/345.37; 156/345.38;
84	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 4842676 A	19890627	84	Process for etch of tungsten	438/711	216/75; 257/E21.311;
85	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 4838990 A	19890613	83	Method for plasma etching tungsten	438/711	204/192.35; 216/75;
86	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 4838984 A	19890613	84	Method for etching films of mercury-cadmium-telluride and zinc s	438/711	257/E21.485; 438/718
87	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 4837113 A	19890606	84	Method for depositing compound from group II-VI	117/103	117/104; 427/562;
88	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 4836905 A	19890606	82	Processing apparatus	204/298.25	118/719; 156/345.51;
89	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 4832779 A	19890523	83	Processing apparatus	156/345.37	216/100; 216/102;
90	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 4832778 A	19890523	83	Processing apparatus for wafers	156/345.31	118/50.1;

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
90	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 4832778 A	19890523	83	Processing apparatus for wafers	156/345.31	118/50.1; 118/620;
91	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 4832777 A	19890523	84	Processing apparatus and method	156/345.37	118/725; 438/715
92	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 4830705 A	19890516	83	Method for etch of GaAs	438/718	204/192.35; 252/79.1;
93	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 4830700 A	19890516	83	Processing apparatus and method	156/345.37	216/21; 216/41;
94	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 4828649 A	19890509	83	Method for etching an aluminum film doped with silicon	438/711	204/192.37; 216/77;
95	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 4822450 A	19890418	84	Processing apparatus and method	438/709	156/345.35; 156/345.36;
96	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 4820378 A	19890411	81	Process for etching silicon nitride selectively to silicon oxide	438/711	204/192.37; 257/E21.252;
97	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 4820377 A	19890411	82	Method for cleanup processing chamber and vacuum process modul	134/1.1	134/1; 156/345.35;
98	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 4818327 A	19890404	82	Wafer processing apparatus	156/345.37	118/620; 204/298.09;
99	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 4818326 A	19890404	83	Processing apparatus	156/345.36	156/345.39; 156/345.53;
100	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 4816098 A	19890328	83	Apparatus for transferring workpieces	156/345.31	118/728; 204/298.25;
101	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 4797718 A	19890110	8	Self-aligned silicon MOS device	257/387	257/623; 257/624;
102	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 4744455 A	19880517		Dispenser and component feeder	198/389	198/396; 198/468.4;
103	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 4371890 A	19830201		Tapering of oxidized polysilicon electrodes	257/291	257/366; 257/749;
104	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 4328511 A	19820504		Taper isolated ram cell without gate	257/261	257/260;